Examination March 14, 2007

Physical electronics, EMI180

(and also valid for "Mikroelektronik för E2 del A, **ETI145**" and "Fysik del C för D2, **FFY171**" – please write the course code for the course you want to be reported for)

Examination occurs in the V-rooms Wednesday March 14 between 08.30 och 12.30. Responsible teacher: Per Lundgren, tel. 772 18 82.

Solutions will be posted on the course homepage (EMI180) Thursday March 15.

Preliminary results will be available on the course homepage no later than Thursday 29/3, and examination of the results is possible on the same day between 10-12 at MC2 (room A504, Valensbandet).

The problems can be solved using the tools of your choice excluding personal interaction and excluding internet access. Select ***only*** three of the four problems to treat and hand in solutions to these three. In order to pass two of the three solutions must show that you are able to apply concepts/models/methods from the course on a problem in a sensible manner (grade 3).

The solutions will be graded either fail, 3, 4 or 5.

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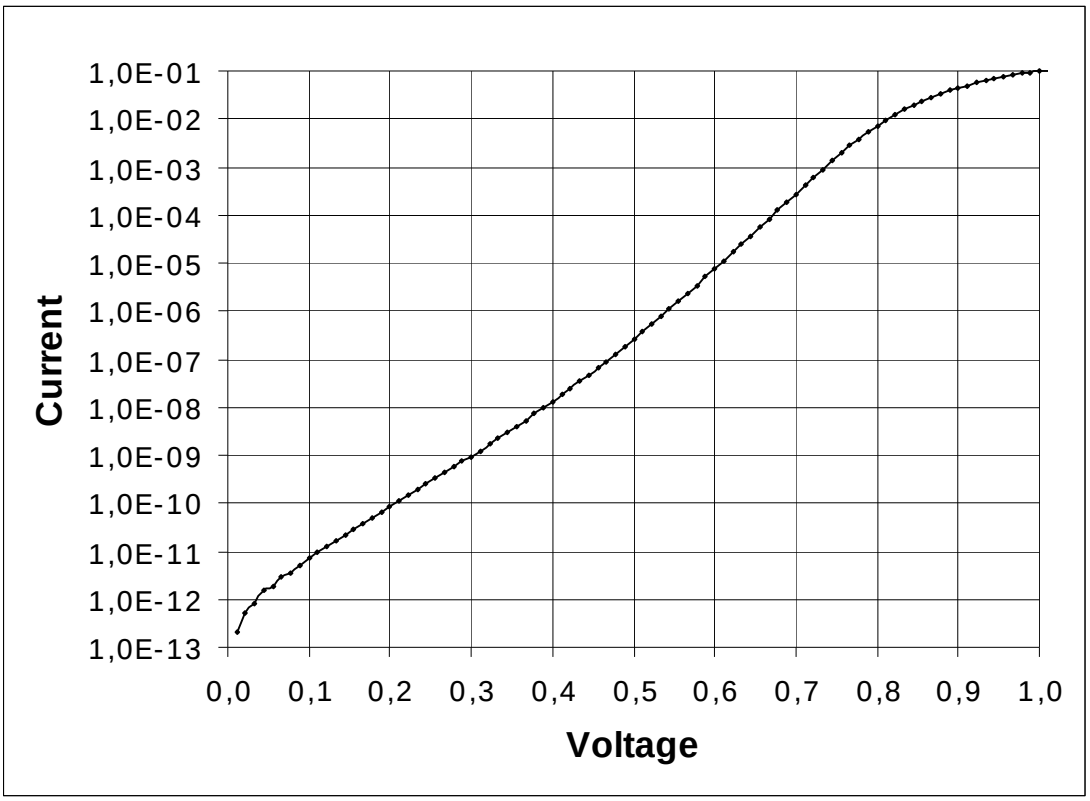
March 2007

Problem 1

In the appended paper ("Transparent amorphous…", Ju-Il Song et al., Applied Physics Letters **90**, 022106, 2007) the authors present electrical characteristics for a MOSFET they have designed for use in flat displays. Describe the significant difference for this device in comparison to crystalline silicon MOSFETs that makes the classification of the transistor as enhancement- or depletion mode difficult. Motivate your classification of this transistor as either enhancement- or depletion mode! Furthermore, you must also correct the error in the authors' analytical description of the saturation current.

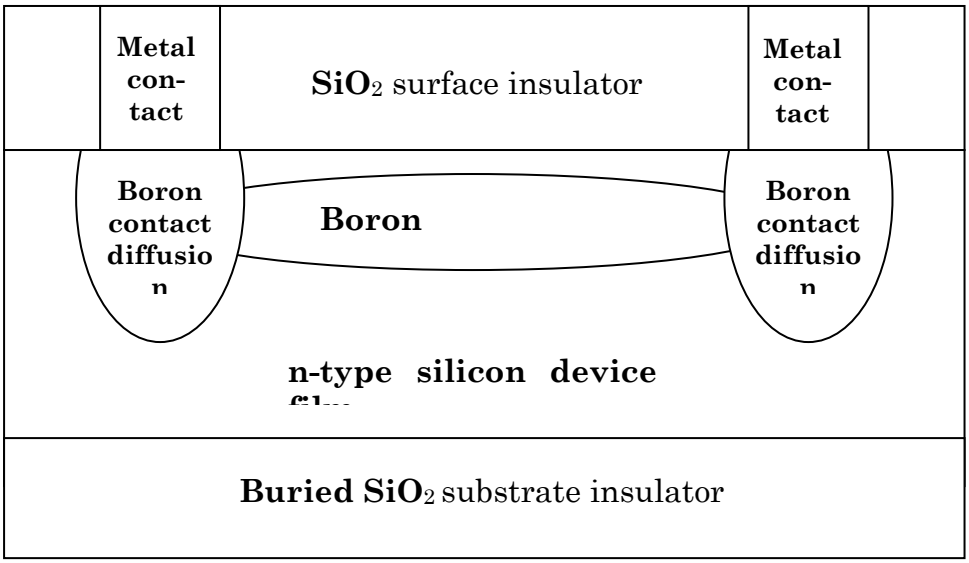
Problem 2

Give a simple piece-wise linear model (defined by "slopes" and "threshold voltages") for the diode with the characteristics in the figure below. The model is to be used to predict the voltage drop over the diode within 100 mV when connected in series with resistances in the range 10-100 MΩ and a voltage source in the range 0-10 V.



Problem 3

The local company Nanofactory are designing and manufacturing force-sensitive probes for use in transmission electron microscopes. In order to sense the deflection of a cantilever, they use resistors defined by boron implantation in a thin n-type silicon layer on top of an insulator. Having a very thin silicon layer is one central feature for this application (to obtain desired mechanical properties). In their first process the resistance of these resistors was found not to scale properly with the width and length of the boron-implanted region – the resistance changed much less than expected when changing these geometries and the absolute value of resistance was lower than expected. From the device cross-section in the figure below for a case similar to that of Nanofactory's, and from the process specification and material analysis data given, suggest an explanation to the observed anomalous behaviour and suggest a method to solve the problem.



Boron implantation: mean depth 1 μm, full-width half maximum of distribution 1 μm, 10^{16} m^{-2} dose (boron atoms).

Boron contact diffusion: depth 2 μm±1 μm, 10^{18} m^{-2} dose

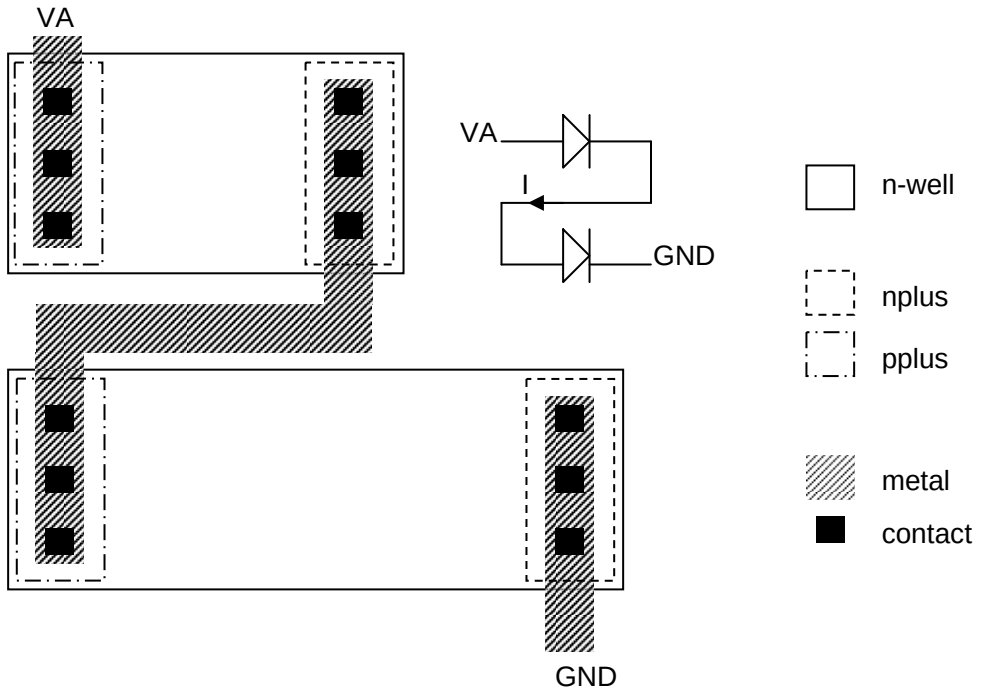
Active silicon layer: thickness 4 μm±1 μm, resistivity: 50 Ωcm

Buried oxide thickness: 100 nm

Segregated boron contamination at the interface between the silicon film and the buried oxide: boron concentration 10^{20}-10^{21} m^{-3}

Problem 4

Two diodes implemented in a p-type substrate CMOS process are connected in series. The layout and circuit schematic are shown here:



Data:

- The n-well sheet resistance is 10 Ω/square.
- The nplus and pplus sheet resistances are 0.2 Ω/square.
- The metal sheet resistance is 0.1 Ω/square.
- The contact resistance is 1 Ω.
- The applied voltage V_A=4 V.

The sheet resistance (Ω/square) is the resistance of a resistor with equal length and width.

Estimate the magnitude of the current *I* flowing through the two diodes!

Layer explanation:

Layer name	Description
n-well	Defines where the n-doped region is in the p-type substrate
nplus	High n-type doping
pplus	High p-type doping
metal	Metal interconnect
contact	Contact between metal and doped layer

Suggested solutions

These suggested solutions are unfortunately NOT designed model suggestions for any particular grading, but simply brief descriptions of one possibility of dealing with the problems in a sensible manner.

Problem 1

First: the error is in the equation where V_{GS} should appear instead of V_{DS}. The significant difference for this device compared to a silicon MOSFET is that the subthreshold slope is significantly altered: more than 2 V per decade change in current compared to less than 100 mV voltage change for a ten fold increase in current for an ordinary silicon MOSFET. For the reported transistor this means that even if you find a threshold voltage by extrapolating the saturation current expression, you still have substantial current for several volts below the threshold voltage, before the current is reduced significantly (several orders of magnitude). I would say that this is a depletion mode transistor, which needs a negative voltage to be really turned off, even though the threshold voltage as determined by conventional means gives a positive value.

Problem 2

First I try to find the limiting cases: which is the highest current that will be occurring in the circuit? This would be the 10 V, 10 MΩ case, resulting in a current close to 1 μA. For that current the voltage over the diode needs to be close to 0,5 V, so a very simple model that would work in that particular case is to say that the threshold voltage of the diode is 0,5 V. At the other end, for low applied voltages there will be a very small current, limited by the diode; as long as the current is below 1 nA the voltage drop over the series resistance will never be higher than 0,1 V, so we could in the low voltage region use a simple model where the diode threshold voltage is 0,3 V (for diode currents up to 1 nA). For diode voltages between 0,3 V and 0,5 V we will have a change of the diode voltage depending on the value of the total applied voltage and on the value of the series resistance. At a current of 100 nA the diode voltage can be taken as as 0,5 V, since it will be somewhere close to 0, 45 V. If we let the diode model increase linearly from 0 A at a voltage of 0,3 V to 100 nA at 0,5 V we would get results that lie within the demands (diode voltage correct within 100 mV).

Problem 3

One explanation for the observed behaviour is that the boron contact diffusions reach down to the buried oxide and make a connection through the segregated boron contamination layer. This will give a parallel resistance that influence the total resistive behaviour in accordance with observations. One remedy is of course to try to eliminate the boron contaminant, but it being there is already a proof that this is not trivial. A better choice is to be more careful when doing the boron contact diffusions

and to use a thicker silicon device film (although this is supposed to be thin for the application in question).

Problem 4

The n-wells will be the main current limiting contribution to the resistance, allowing for a voltage drop of 0,7 V over each forward biased diode. Counting “squares” for the n-well, I find approximately 3, so we end up with some 2,6 V over 30 Ω or approximately 0,1 A.