Examination January 17 2007

Physical electronics, EMI180

Examination occurs in the V-rooms Wednesday January 17 between 08.30 och 12.30. Responsible teacher: Lennart Lundgren, tel. 772 18 34.

Solutions will be posted on the course homepage Thursday January 18.

Preliminary results will be available on the course homepage no later than Thursday 25/1, and examination of the results is possible on the same day between 10-12 at MC2 (room B509).

The problems can be solved using the tools of your choice excluding personal interaction and excluding internet access. Select three of the four problems to treat and hand in solutions to these three. In order to pass two of the three solutions must show that you are able to apply concepts/models/methods from the course on a problem in a sensible manner (grade 3).

The solutions will be graded either fail, 3, 4 or 5.

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Problem 1

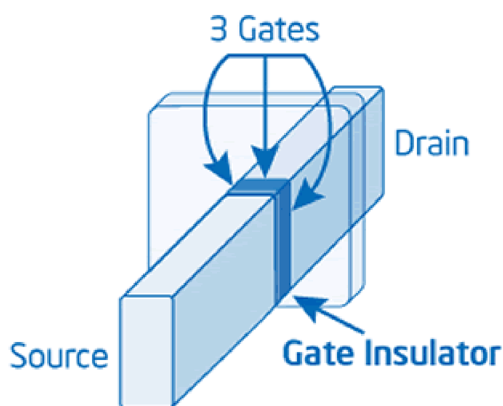
In the appended paper the authors present a schematic energy band diagram for one of the material structures in their investigation (ITO/PF samples). They conduct the same experiments also on ITO/PEDOT samples. Make a matching energy band diagram for the ITO/PEDOT samples based on the findings in the paper. For higher grading (4 or 5) also make an energy band diagram for only the ITO film without polymer coating and comment on the reason for and implications of the differences with and without polymer coating.

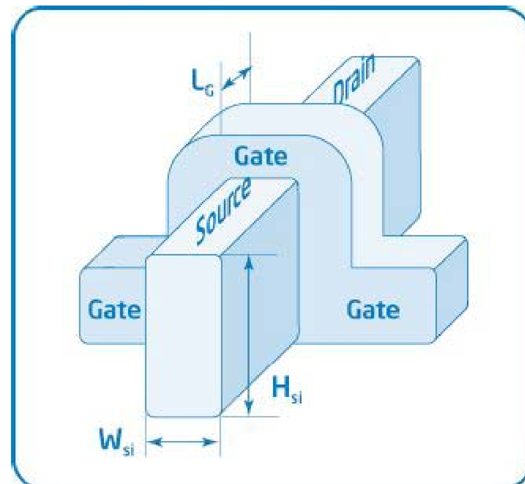
Problem 2

Calculate the maximum voltage sensitivity (largest possible absolute current density [A/m^2] change per volt) that you can achieve for forward biased pn-junction devices in silicon technology.

Problem 3

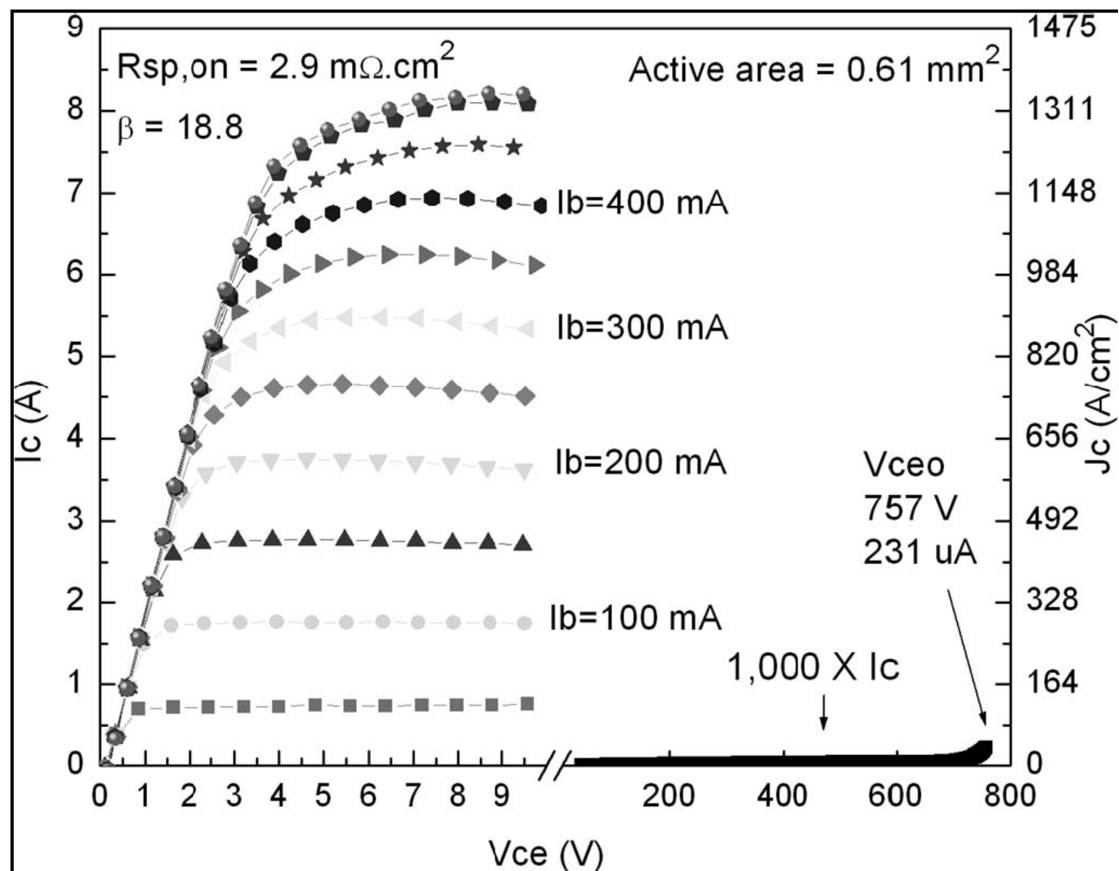
The images below are from INTEL's home pages, where they describe their recent work on "tri-gate" transistors. Make a (motivated) quantitative estimate of the performance enhancement achievable with this transistor design compared to ordinary planar CMOS transistors.





Problem 4

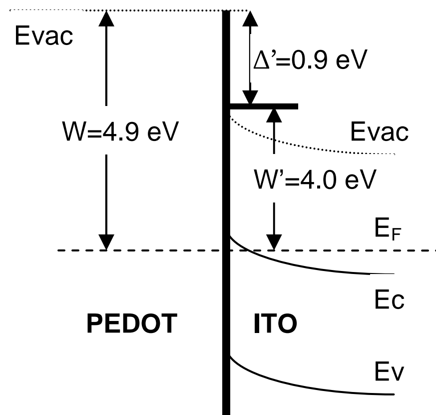
The figure below is from a recent publication in IEEE Electron Device Letters, vol. 27, no. 5, May 2006 by J. Zhang and co-workers. What are your conjectures regarding the fabrication/design of this device in terms of reasonable quantitative estimates for relevant design parameters, given the information in the figure?

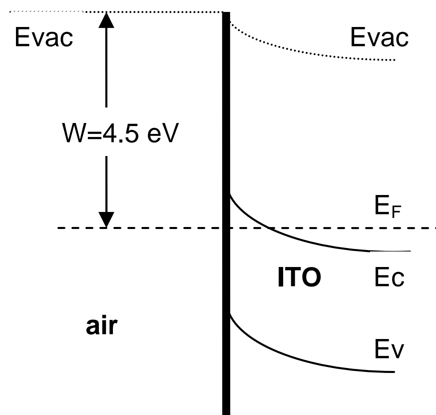


Suggested solutions

These suggested solutions are unfortunately NOT good model suggestions for any particular grading, but simply brief descriptions of one possibility of dealing with the problems in a sensible manner.

Problem 1





The change induced by the polymer can be imaged as a very thin dipole layer, where there will be a voltage (potential) drop Δ (0.7 eV for PF and 0.4 eV for PEDOT). The authors argue that that image is inaccurate; in addition there will be a substantial change in the surface potential (band bending), e. g. induced by changes in the amount of fixed charge at the interface. From the authors description, the dipole induced contribution is the same for both coatings (0.9 eV), and it is the difference in band bending (fixed interface charge) that makes up the 0.3 eV difference in measured work function for the two different coatings.

Problem 2

Using the ideal diode equation:

$$J = J_0\left(e^{\frac{qV}{kT}} - 1\right),$$

we will get the following expression for the current change for a change in voltage (looking at high enough forward bias to neglect "-1"):

$$\frac{dJ}{dV} \approx \frac{q}{kT} \cdot J \, .$$

According to this expression we would like to have as high current density as possible, but when we increase the current in the ideal diode equation, we will run into the case where the current limitation will be set by the resistive n- and p-regions outside the actual junction. In that case the voltage sensitivity will simply be determined by the conductivity of the lowest doped region outside the junction (the series resistance):

$\frac{dJ}{dV} \approx \frac{qN\mu}{l}$, where l is the length of the low-doped region.

Now, to maximize the sensitivity we clearly need to have high mobility, high doping, and a short low-doped region. According to Figure 3.8 in Pierret we can achieve a conductivity of approximately 10^4 S/m for dopings of 10^{25} m^{-3}, and with a (very short) length (substrate thickness) of 10 μm we will arrive at a maximum voltage sensitivity of 10^9 Sm^{-2} (assuming room temperature operation).

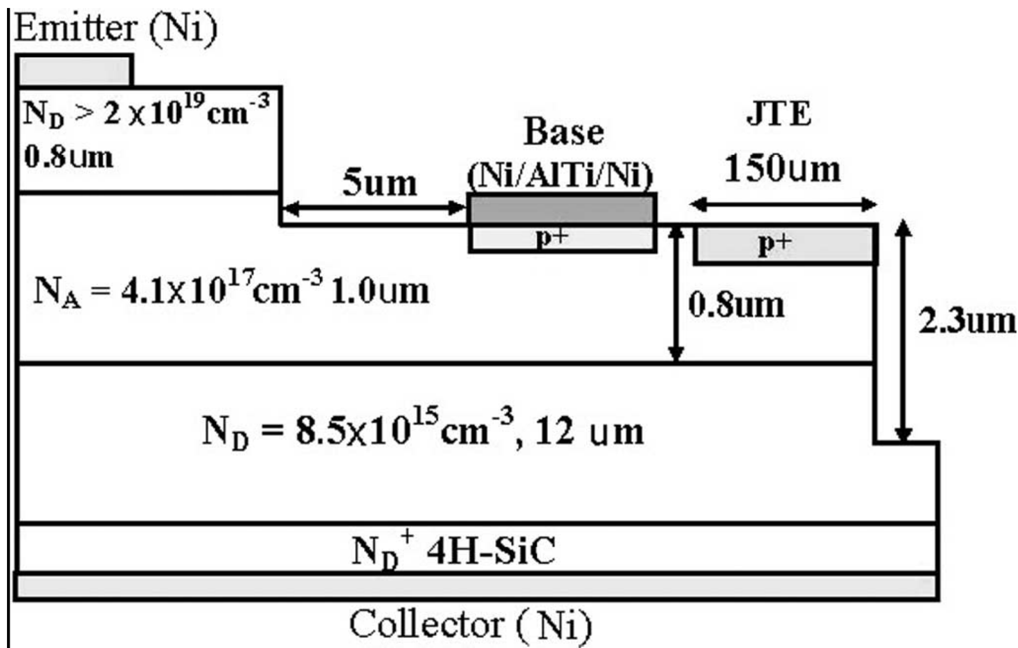
Problem 3

Quoting Intel: "Intel's tri-gate technology surrounds the channel on three of four sides, making it significantly more power efficient than…planar...transistor technology." The enhanced power efficiency comes from the high attainable ratio between "on" and "off" currents for the tri-gate design. Scaling up the current for a planar device by e. g. scaling down the channel length (to increase speed) will give increases both for the saturation current and for the current when the device is supposed to be "off". Since power management is a critical issue (you are not allowed to consume more than a certain amount of power on the chip), it is highly desirable to minimize all possible power dissipation. With the tri-gate design you can enhance the saturation current without enhancing the unwanted leakage currents. One way of explaining this is to regard the tri-gate as a widening of the gate without increased device footprint (planar area on the chip) and without increased leakage paths through the substrate. Assuming that the figure is reasonable to scale, the gate width is increased with a factor of 5, which would imply a five-fold performance enhancement. In reality Intel achieves an increase in on/off ratio with the tri-gate design of approximately 50% compared to planar CMOS.

Problem 4

From the quoted paper with the original figure:

"Silicon carbide electronic devices have received more and more attention recently due to their wide bandgap material properties and fast-maturing technologies. 4H-SiC (Eg = 3.26 eV) bipolar junction transistor (BJT) is an important switching device for high-power and high-temperature applications. It is an intrinsically normally OFF device, does not have gate oxide problems, and conducts high current with a low forward voltage drop. For a power 4H-SiC BJT device, high blocking voltage, low ON-state resistance and high current gain, are desirable for better efficiency."



To estimate dimensions and doping concentrations I would have assumed that the device was a bipolar transistor made in silicon (which is obviously is not according to the paper). The breakdown voltage indicates a low doped collector of 10^{20} m^{-3} (e. g. from Figure 6.11 in Pierret), and I would have guessed n-type doping in the collector. The low on-resistance of 0.5 Ω or so would then have to imply a collector thickness (l) of no more than 0,5 μm from using:

$$R = \frac{l}{q\mu N_D A}.$$

Now that length does NOT fit with a 757 V breakdown voltage, since the depletion width at 757 V is much larger, so my design obviously will not work. I would then have to consider a different material which could give either much higher mobility to allow a thicker collector or which gives a much higher breakdown voltage for a particular doping. SiC gives both.