Examination 18 december 2006

Physical electronics, EMI180

Examination occurs in the VV-rooms Monday December 18 between 08.30 och 12.30. Responsible teacher: Lennart Lundgren, tel. 772 18 34.

Solutions will be posted on the course homepage Tuesday December 19.

Preliminary results will be available on the course homepage no later than Friday 22/12., and examination of the results is possible on the same day between 10-12 at MC2 (room B509).

The problems can be solved using the tools of your choice excluding personal interaction. Select three of the four problems to treat and hand in solutions to these three. In order to pass all three must be treated satisfactorily according to the criterion: being able to apply concepts/models/methods from the course on a problem in a sensible manner (grade 3).

The solutions will be graded either fail, 3, 4 or 5.

Chalmers University of Technology

Department of Microtechnology and Nanoscience

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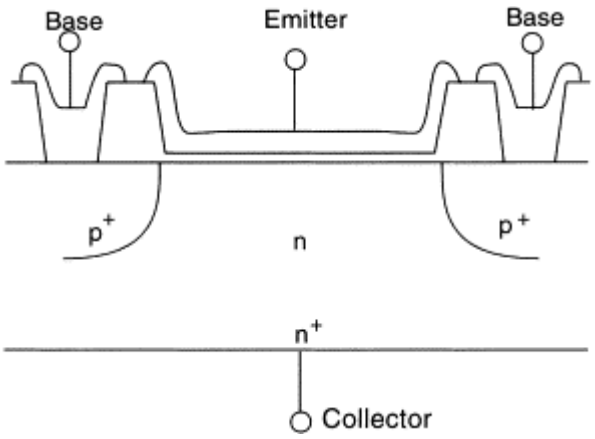
Problem 1

Motivate your suggestion of a small-signal equivalent circuit for the device in the cross-sectional figure below, assuming that it is in active operation. This is a bipolar device for which MC2 at Chalmers has world record in current gain (collector current over base current). Between the aluminum emitter and the silicon n-substrate there is an ultra thin (2 nm) silicon dioxide layer.



Problem 2

Calculate the maximum relative capacitance difference that you can achieve by altering the reverse bias for pn-junction devices in silicon technology.

Problem 3

In the appended paper the authors present two transistors based on a polymer material. Motivate your choice of one of these for the design of a resistively loaded inverter, and describe your design.

Problem 4

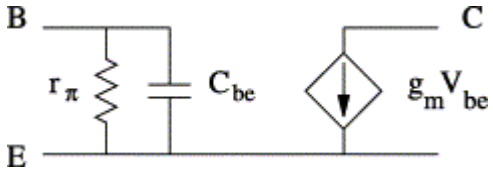
For the transistor with PEDOT contacts for source and drain in the same paper as above, calculate the hole mobility using its on-conductance (dI_{ds}/dV_d) and comment on the result in comparison to the mobility value presented in the paper from measurements in saturation.

Suggested solutions

These suggested solutions are unfortunately NOT good model suggestions for high grading, but simply brief descriptions of one possibility of dealing with the problems in a sensible manner.

Problem 1

One small-signal model suggested by Erik Aderstedt who worked with these Tunnel Emitter Transistors at MC2 is as follows:



The current through the thin silicondioxide layer consists of electrons going from emitter to collector and holes coming from the base going out to the emitter. By changing the base-emitter voltage the amount of holes available in the substrate under the oxide changes (charging/discharging the base-emitter capacitor), and this alters the voltage drop over the oxide, which controls the electron tunnelling current through the oxide. The device gives current gain mainly because there is a significant difference in tunnelling transparency for electrons and holes in the oxide – the input resistance r_π is high.

Problem 2

We look for the ratio of maximum to minimum capacitance, which should be the same as the ratio of maximum to minimum space-charge region width. The parameters we can control (besides the applied voltage) are doping and temperature. If assuming room temperature operation, we are left with changing the doping. Further assuming p+-n junctions, we limit the discussion to different n-doping levels. A thin space-charge region is achieved at low bias (0 V) and high doping, and wide space-charge regions are achieved by high negative biasing and low doping. We could probably do well by having high doping close to the actual junction, and then let the doping decrease as we go further in to the n-material. To simplify I will assume constant n-doping, and then choose whether to use high or low doping. The minimum space-charge width is given by:

$w_{\min} = \sqrt{\frac{2\varepsilon V_0}{qN}}$, from Poisson's equation.

V_0 is the contact potential (near 0,7 V for any doping).

The maximum space-charge width can be set by the breakdown field, since at breakdown in the reverse direction of a pn-junction we have:

$w_{\max} = \frac{\varepsilon E_{BD}}{qN}$, from Maxwell's first relation between E-field and charge.

The breakdown field (E_{BD} or E_{CR}) is approximately 10^8 V/m for silicon. Dividing the expression for space-charge width we end up with:

$$\frac{w_{\max}}{w_{\min}} = \sqrt{\frac{\varepsilon E_{BD}^2}{2V_0 qN}},$$

Where we see that we want to use as small a doping as possible. It is difficult to have doping levels lower than 10^{18} m^{-3}, so I pick this value and get the maximum relative capacitance difference (ratio of capacitances) to be approximately 2000, but this will demand a very thick silicon sample (1 dm) and also very large area to get a measurable capacitance that is not drowned by parasitics!

Problem 3

I choose the device with gold electrodes and connect the drain of the transistor to -30 V (source grounded) via a load resistor of 30 MΩ. This will give me an output voltage of a magnitude which is less than -10 V for high input voltage (magnitude larger than -25 V), and an input of lower magnitude than -10 V will give an output voltage very close to -30 V. For the PEDOT-contacted devices it will be difficult to maintain a large swing between high and low voltage level in a resistively loaded inverter configuration. If we assume a 300 MΩ resistive load, a high input (magnitude larger than -25 V) would yield an output no less in magnitude than -10 V. Having that as input for a second inverter will yield an output of -20 V which is too low to be regarded as a "high" level (magnitude larger than -25 V in our example).

Problem 4

Taking data from Figure 3(a) we get a current of 0,02 mA at 3 V applied drain voltage resulting in G_{ON}=6,7·10^{-9} A/V. The transistor dimensions are W=1 mm and L=100 μm. The oxide capacitance is found from $C_{ox}=\varepsilon/t=3{,}6.\varepsilon_0/500\text{nm}=6{,}4\cdot10^{-5}$ F/m^2.

We use $G_{ON}=W/L*\mu C_{ox}(V_{GS}-V_T)$, from Shockley's transistor model to calculate the mobility. From Figure 4a we see a threshold voltage between 2 and 5 V. Using the numbers above we arrive at a mobility of 3·10^{-3} cm^2/Vs which is in accordance with the authors derivation in saturation given as (2,6± 0,6)*10^{-3} cm^2/Vs. (This is an extremely poor mobility; compare with silicon hole mobility (which is not high to begin with) of 500 cm^2/Vs).